UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,073	01/20/2004	Simon C. Steely JR.	200313630-1	3181

22879 7590 03/29/2007

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
CAMPOS, YAIMA	
ART UNIT	**PAPER NUMBER**
2185	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/29/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/761,073	STEELY ET AL.	
	Examiner	Art Unit	
	Yaima Campos	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

RESPONSE TO AMENDMENT

1. The examiner acknowledges the applicant's submission of the amendment dated December 20, 2006. At this point claims 1, 16, 21, 27, 31 and 34 have been amended, and no claims have been cancelled. There are 40 claims pending in the application; there are 7 independent claims and 33 dependent claims, all of which are ready for examination by the examiner.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 1-9, 12-14, 16-22, 25-29, 31-37 and 39-40** are rejected under 35 U.S.C. 102(b) as being anticipated by Arimilli et al. (US 2002/0129211).

4. As per **claim 1**, Arimilli discloses

A system comprising:

"a first node that provides a source broadcast request for data, the first node being operable to respond in a first manner to other source broadcast requests for the data while the source broadcast request for the data is pending at the first node;" as **["a plurality of agents coupled to an interconnect...in response to snooping the transaction, a second agent provides a snoop response indicating that the second agent has a pending conflict store request" and explains**

that "master 26 prevents access to the target cache line by other agents 10 by means of appropriate snoop responses until the store into cache array 24 is completed" (Pages 1-2, Paragraph 0012; Page 4, Paragraphs 0035-0038)]

"the first node being operable to respond in a second manner to the other source broadcast requests for the data in response to receiving an ownership data response at the first node" **[With respect to this limitation, Arimilli discloses "and a coherency decision point provides a snoop response granting the first agent ownership of the data" (Pages 1-2, Paragraph 0012; Page 4, Paragraphs 0035-0038)]**

the ownership data response comprising a copy of the data **["The one or more shared cache coherency states may optionally include a shared-owner state that designates a single owner of a potentially shared cache line" (Page 2, Par. 0024) and explains that "master 26 of a first agent, for example, processor complex 10a issues a modifying transaction 150a (i.e., Dclaim or RWITM)" (Page 3, Par. 0029) wherein this processor is granted ownership of the cache line and is designated as OWNER or OWNER_CU (See Table III in Page 6) wherein "The RWITM transaction requests that the initiating agent be provided an up-to-date copy of a target cache line and that other agents invalidate their copies of the cache line, if any" (Page 1, Par. 0006); therefore, disclosing "an ownership response comprising a copy of the data"]**.

Arimilli explicitly discloses **["master 26" in the system receives store requests for cache lines wherein "master 26 handles the store request according to the coherency state associated with the request address in the cache directory 22... if, however, cache directory 22 indicates the target cache line identified by the request address is invalid... master 26**

issuing a RWITM transaction on system bus 12 to obtain a copy of the cache line from another agent 10 for modification" (Page 4, Par. 0035); therefore, as master issues a "RWITM" transaction for data and data is transferred from an agent that has previously modified a cache line to the agent that intends to modify this cache line in order to provide this agent requesting ownership the most-current data in the system, master is issuing an ownership response request comprising a copy of the data as claimed by Applicant].

5. As per **claim 2**, Arimilli discloses the system of claim 1, **[See rejection to claim 1 above]** "wherein the ownership data response comprises an indication to the first node that the data associated with the ownership data response comprises migratory data" **[Arimilli discloses this concept as "master receives a store request from processor 16... master 26 sets its Dclaim pending flag and initiates a Dclaim transaction on system bus 12 to obtain ownership of the target cache line from the CDP" wherein "a shared state (defined herein as any state indicating that identical data may be held in another cache14)" (Figure 3A; Page 4, Paragraphs 0035-0036)]**.

6. As per **claims 3 and 4**, Arimilli discloses the system of claim 2, **[See rejection to claim 2 above]** "wherein the migratory data comprises a cache ordering point for serializing source broadcast requests for the data, the cache ordering point migrating to the first node from a node that provides the ownership data response" **[Arimilli discloses this concept as "in addition, to maintain coherency, master 26 performs clean-up operations to invalidate other (now stale) copies of the target cache line, if any, held by other agents 10, and further, to ensure that the associated snooper 28 provides snoop responses informing masters 26, if any, that lost the arbitration to downgrade their Dclaim transactions to RWITM transactions... while**

master 26 is issuing these Kill transactions, the associated snooper 28 provides NACK snoop responses to Dclaim transactions of losing masters 26 that did not receive a NACK snoop response" (Page 4, Paragraph 0038; Table I)].

7. As per **claim 5**, Arimilli discloses the system of claim 1, **[See rejection to claim 1 above]** wherein "the source broadcast request from the first node comprises a source broadcast read request, the first node, when responding in the first manner, provides a first response to the other source broadcast requests for the data indicating that the first node has a conflicting read request for the data" **[Arimilli discloses this concept as "coordination of accesses satisfied by multiple possible data sources to ensure that read and write accesses to each system memory address are ordered such that agents requesting read access receive correct data" (Page 1, Paragraph 0005) and explains that "master 26 prevents access to the target cache line by other agents 10 by means of appropriate snoop responses until the store into cache array 24 is completed" wherein "a master intends to modify a shared cache line held in its associated cache and that the other agents should invalidate their cached copies of the cache line... master 26 performs clean-up operations to invalidate other (now stale) copies of the target cache line held by other agents 10" (Pages 1-2, Paragraph 0012; Page 4, Paragraphs 0035-0038)]**.

8. As per **claim 6**, Arimilli discloses the system of claim 5, **[See rejection to claim 5 above]** further comprising "a second node that provides one of the other source broadcast requests for the data and receives the first response from the first node, the second node being operative to fill a shared copy of data received from a third node in response to the one of the other source broadcast requests for the data" **[With respect to this limitation, Arimilli discloses**

having "agents 10" (Figure 1) and explains that "the first agent is permitted to modify data. To maintain coherency, the first agent also invalidates other cached copies of the data, if any" (Pages 1-2, Paragraph 0012) wherein a single-owner may modify a cache line at a time (Page 2, Paragraph 0024) wherein "a conflict arises if during interval 160, the master 26 of a second agent 10 (and possibly one or more agents 10) develops, or has previously developed and manifests, at any time during interval 160 an intention to modify the target cache line" (Page 3, Paragraph 0029)|.

9. As per **claim 7**, Arimilli discloses the system of claim 5, **[See rejection to claim 5 above]** further comprising "a second node that provides one of the other source broadcast requests for the data and receives the first response from the first node, the second node being operative to fill a copy of data received from a home node for the data" **[The rationale in the rejection of claim 6 is incorporated herein]**.

10. As per **claim 8**, Arimilli discloses the system of claim 1, **[See rejection to claim 1 above]** wherein "the first node, when responding in the second manner, provides a second response to the other source broadcast requests for the data indicating that the source broadcast request from the first node is a conflicting request for the data and that migration of the data to the first node is in progress" **[With respect to this limitation, Armilli discloses "response logic 30 combines the snoop response of the CDP with the snoop responses of the other agents 10 to produce a combined response. In the case of multiple conflicting requests shown in FIG. 2, the combined response informs an agent 10 that issued a transaction whether or not it won the arbitration performed by the CDP and is the new owner of the target cache line... the granting CDP protects ownership of target cache line by providing snoop responses**

denying ownership to other agents that issue conflicting responses" (Pages 3-4, Paragraphs 0032-0033) and explains that "master 26 prevents access to the target cache line by other agents 10 by means of appropriate snoop responses until the store into the cache array 24 is completed" (Page 4, Paragraph 0036)].

11. As per **claim 9**, Arimilli discloses the system of claim 8, **[See rejection to claim 8 above]** further comprising "a second node that provides one of the other source broadcast requests for the data and receives the second response from the first node, the second node being operative to employ a copy of the data received from a third node for only a single use" **[Arimilli discloses this concept as "coherency protocols typically require that only a single agent can own each line at any given time for purposes of modification" (Page 3, Paragraph 0033)]**.

12. As per **claims 12 and 17**, Arimilli discloses the system of claims 1 and 16, **[See rejection to claim 1 above and rejection to claim 16 bellow]** wherein "the first node employs an invalidate line command to other nodes of the system to remove incorrect copies of the data and any stale copies of the data cached at the other nodes of the system". **[Arimilli discloses this limitation as "to maintain coherency, master 26 performs clean-up operations to invalidate other (now stale) copies of the target cache line, if any, held by other agents 10... master 26 invalidates other copies of the target cache line by issuing high-priority Kill transactions on system bus 12 until all other agents provide Null snoop responses indicating that other copies of the cache line have been invalidated" (Page 4, Paragraph 0038)]**.

13. As per **claim 13**, Arimilli discloses the system of claim 1, **[See rejection to claim 1 above]** wherein the source broadcast request provided by the first node is broadcast using a

source broadcast cache coherency protocol **[Arimilli discloses this concept as agents snoop to use resources (Pages 1-2, Paragraphs 0011-0012; Figure 4)]**.

14. As per **claim 14**, Arimilli discloses the system of claim 1, **[See rejection to claim 1 above]** wherein "the first node defines a processor having an associated cache, the associated cache of the processor comprising a plurality of cache lines, each cache line having a respective tag address that identifies associated data and each cache line having state information that indicates a state of the associated data for the respective cache line," **[With respect to this limitation, Arimilli discloses cache lines having tag fields (Pages 2-3, Paragraphs 0023 and 0025; Figure 1)]**

"the processor being capable of communicating with other nodes of the system through an interconnect," **[Arimilli discloses this limitation as "a plurality of agents coupled to an interconnect" (Page 1, Paragraph 0012; Figure 1)]**

"the system further comprising a cache controller associated with the processor, the cache controller being operative to manage data requests and responses for the associated cache of the processor, the cache controller effecting state transitions associated with the data in the associated cache of the processor based on the data requests and responses for the associated cache of the processor" **[Arimilli discloses this limitation as "master 26" and "snooper 28" (Pages 2-3; Paragraphs 0024-0026; Figure 1) wherein "in addition, to maintain coherency, master 26 performs clean-up operations to invalidate other (now stale) copies of the target cache line, if any, held by other agents" and explains that "while master 26 is issuing these Kill transactions, the associated snooper 28 provides NACK snoop responses to Dclaim**

transactions of losing masters 26 that did not receive an NACK snoop response" (Page 4, Paragraph 0038)].

15. As per **claim 16**, Arimilli discloses

A multi-processor network comprising: as **["data processing system 8" (Figure 1)]**

"a source processor node that provides a source broadcast read request for data; the source processor node issuing an invalidate line command to other processor nodes of the system in response to receiving a data response that transfers a cache ordering point for the data to the source processor node" **[Arimilli discloses this concept as "a plurality of agents coupled to an interconnect...in response to snooping the transaction, a second agent provides a snoop response indicating that the second agent has a pending conflict store request" and explains that "master 26 prevents access to the target cache line by other agents 10 by means of appropriate snoop responses until the store into cache array 24 is completed" (Pages 1-2, Paragraph 0012; Page 4, Paragraphs 0035-0038) and explains "and a coherency decision point provides a snoop response granting the first agent ownership of the data" (Pages 1-2, Paragraph 0012; Page 4, Paragraphs 0035-0038) wherein "a conflict arises if, during interval 160, the master 26 of a second agent 10 (and possibly one or more additional agents 10) develops, or has previously developed and manifests at any time during interval 160 an intention to modify the target cache line" (Page 3, Paragraph 0029) "master 26 invalidates other copies of the target cache line by issuing high-priority Kill transactions... while master 26 is issuing these Kill transactions, the associated snooper 28 provides NACK snoop responses to Dclaim transactions of losing masters 26 that did not receive an NACK snoop response" (Page 4, Paragraph 0038)]**

"the first node being operable to respond in a second manner to the other source broadcast requests for the data in response to receiving an ownership data response at the first node" **[With respect to this limitation, Arimilli discloses "and a coherency decision point provides a snoop response granting the first agent ownership of the data" (Pages 1-2, Paragraph 0012; Page 4, Paragraphs 0035-0038)]**

the ownership data response comprising a copy of the data **["The one or more shared cache coherency states may optionally include a shared-owner state that designates a single owner of a potentially shared cache line" (Page 2, Par. 0024) and explains that "master 26 of a first agent, for example, processor complex 10a issues a modifying transaction 150a (i.e., Dclaim or RWITM)" (Page 3, Par. 0029) wherein this processor is granted ownership of the cache line and is designated as OWNER or OWNER_CU (See Table III in Page 6) wherein "The RWITM transaction requests that the initiating agent be provided an up-to-date copy of a target cache line and that other agents invalidate their copies of the cache line, if any" (Page 1, Par. 0006); therefore, disclosing "an ownership response comprising a copy of the data"]**.

Arimilli explicitly discloses **["master 26" in the system receives store requests for cache lines wherein "master 26 handles the store request according to the coherency state associated with the request address in the cache directory 22... if, however, cache directory 22 indicates the target cache line identified by the request address is invalid... master 26 issuing a RWITM transaction on system bus 12 to obtain a copy of the cache line from another agent 10 for modification" (Page 4, Par. 0035); therefore, as master issues a "RWITM" transaction for data and data is transferred from an agent that has previously**

modified a cache line to the agent that intends to modify this cache line in order to provide this agent requesting ownership the most-current data in the system, master is issuing an ownership response request comprising a copy of the data as claimed by Applicant].

16. As per **claims 18 and 26**, Arimilli discloses the multi-processor network of claim 16, **[See rejection to claim 16 above]** wherein "the source processor node is operative to provide a first conflict response to source broadcast requests for the data from the other processor nodes prior to receiving the data response that transfers the cache ordering point for the data to the source processor node, the source processor node being operative to provide a second conflict response to at least one source broadcast request for the data from at least one of the other processor nodes in response to the source processor node receiving a conflict response and receiving the data response that transfers the cache ordering point for the data to the source processor node" **[Arimilli discloses this concept as "a plurality of agents coupled to an interconnect...in response to snooping the transaction, a second agent provides a snoop response indicating that the second agent has a pending conflict store request" and explains that "master 26 prevents access to the target cache line by other agents 10 by means of appropriate snoop responses until the store into cache array 24 is completed" (Pages 1-2, Paragraph 0012; Page 4, Paragraphs 0035-0038) and explains "and a coherency decision point provides a snoop response granting the first agent ownership of the data" (Pages 1-2, Paragraph 0012; Page 4, Paragraphs 0035-0038) wherein "a conflict arises if, during interval 160, the master 26 of a second agent 10 (and possibly one or more additional agents 10) develops, or has previously developed and manifests at any time during interval 160 an intention to modify the target cache line" (Page 3, Paragraph 0029) "master 26**

invalidates other copies of the target cache line by issuing high-priority Kill transactions... while master 26 is issuing these Kill transactions, the associated snooper 28 provides NACK snoop responses to Dclaim transactions of losing masters 26 that did not receive an NACK snoop response" (Page 4, Paragraph 0038)].

17. As per **claim 19**, Arimilli discloses the system of claim 18, **[See rejection to claim 18 above]** wherein "the source processor node provides the first response to the source broadcast requests for the data from the other processor nodes when the source processor node has a pending conflicting read request for the data" **[The rationale of claim 5 is herein incorporated]**.

18. As per **claims 20 and 27-28**, Arimilli discloses the system of claim 19, **[See rejection to claim 19 above]** wherein "the other processor nodes receiving the first response from the source processor node are operative to fill a copy of the data received from at least one of the other processor nodes and from system memory" **[The rationale of claim 6 is herein incorporated]**.

19. As per **claim 21**, Arimilli discloses the system of claim 18, **[See rejection to claim 18 above]** wherein "the source processor node provides the second response in response to the source processor node receiving a request for the data that conflicts with the source broadcast request for the data after migration of the copy of the data to the source processor node has begun" **[Arimilli discloses this concept as "while master 26 is issuing these Kill transactions, the associated snooper 28 provides NACK snoop responses to Dclaim transactions of losing masters 26 that did not receive an NACK snoop response during interval 12" (Page 4, Paragraph 0038)]**. Arimilli also discloses **["The one or more shared cache coherency states may optionally include a shared-owner state that designates a single owner of a potentially**

shared cache line" (Page 2, Par. 0024) and explains that "master 26 of a first agent, for example, processor complex 10a issues a modifying transaction 150a (i.e., Dclaim or RWITM)" (Page 3, Par. 0029) wherein this processor is granted ownership of the cache line and is designated as OWNER or OWNER_CU (See Table III in Page 6) wherein "The RWITM transaction requests that the initiating agent be provided an up-to-date copy of a target cache line and that other agents invalidate their copies of the cache line, if any" (Page 1, Par. 0006); therefore, disclosing "an ownership response comprising a copy of the data"].

Arimilli explicitly discloses **["master 26" in the system receives store requests for cache lines wherein "master 26 handles the store request according to the coherency state associated with the request address in the cache directory 22... if, however, cache directory 22 indicates the target cache line identified by the request address is invalid... master 26 issuing a RWITM transaction on system bus 12 to obtain a copy of the cache line from another agent 10 for modification" (Page 4, Par. 0035); therefore, as master issues a "RWITM" transaction for data and data is transferred from an agent that has previously modified a cache line to the agent that intends to modify this cache line in order to provide this agent requesting ownership the most-current data in the system, master is issuing an ownership response request comprising a copy of the data as claimed by Applicant].**

20.

21. As per **claims 22 and 29**, Arimilli discloses the system of claim 21, **[See rejection to claim 21 above]** wherein "one of the other processor nodes comprises a second processor node that provides a respective one of the other source broadcast requests for the data and receives the

second response from the first node, the second processor node being operative to employ a copy of the data received from a third node for a single use" **[The rationale of claim 9 is herein incorporated]**.

22. As per **claim 25**, Arimilli discloses "A system comprising: means for broadcasting a source broadcast request for data from a first node; and means for issuing from the first node an invalidate line command to other nodes of the system in response to receiving a conflict response from at least one other node in the system and a data response transferring a cache ordering point for the data to the first node" **[The rationale in the rejection of claim 16 is herein incorporated]**.

23. As per **claim 31**, Arimilli discloses "A system comprising: means for broadcasting a source broadcast request for data from a first node; means for providing from the first node a first conflict response to other source broadcast requests for the data from other nodes while the source broadcast for the data is pending at the first node; and means for providing a second conflict response to the other source broadcast requests for the data from the other nodes after receiving an ownership data response at the first node while the source broadcast for the data is pending at the first node" **[The rationale in the rejection of claim 1 is herein incorporated. Arimilli further explains that "a conflict arises if, during interval 160, the master 26 of a second agent 10 (and possibly one or more additional agents 10) develops, or has previously developed and manifests at any time during interval 160 an intention to modify the target cache line" (Page 3, Paragraph 0029) "master 26 invalidates other copies of the target cache line by issuing high-priority Kill transactions... while master 26 is issuing these Kill transactions, the associated snooper 28 provides NACK snoop responses to Dclaim**

transactions of losing masters 26 that did not receive an NACK snoop response" (Page 4, Paragraph 0038)]

the ownership data response comprising a copy of the data **["The one or more shared cache coherency states may optionally include a shared-owner state that designates a single owner of a potentially shared cache line" (Page 2, Par. 0024) and explains that "master 26 of a first agent, for example, processor complex 10a issues a modifying transaction 150a (i.e., Dclaim or RWITM)" (Page 3, Par. 0029) wherein this processor is granted ownership of the cache line and is designated as OWNER or OWNER_CU (See Table III in Page 6) wherein "The RWITM transaction requests that the initiating agent be provided an up-to-date copy of a target cache line and that other agents invalidate their copies of the cache line, if any" (Page 1, Par. 0006); therefore, disclosing "an ownership response comprising a copy of the data"]**.

Arimilli explicitly discloses **["master 26" in the system receives store requests for cache lines wherein "master 26 handles the store request according to the coherency state associated with the request address in the cache directory 22... if, however, cache directory 22 indicates the target cache line identified by the request address is invalid... master 26 issuing a RWITM transaction on system bus 12 to obtain a copy of the cache line from another agent 10 for modification" (Page 4, Par. 0035); therefore, as master issues a "RWITM" transaction for data and data is transferred from an agent that has previously modified a cache line to the agent that intends to modify this cache line in order to provide this agent requesting ownership the most-current data in the system, master is issuing an ownership response request comprising a copy of the data as claimed by Applicant]**.

24. As per **claim 32**, Arimilli discloses the system of claim 31, **[See rejection to claim 31 above]** further comprising "means for cleaning-up incorrect copies of the data and stale copies of the data filled at other nodes of the system in response to receiving the ownership data response at the first node" **[With respect to this limitation, Arimilli discloses "master 26 must perform clean-up operations to ensure coherency" (Page 7, Paragraphs 0038 and 0058)]**.

25. As per **claim 33**, Arimilli discloses the system of claim 31, **[See rejection to claim 31 above]** further comprising "means for issuing an invalidate line command to the other nodes of the system in response to receiving the ownership data response at the first node" **[With respect to this limitation, Arimilli discloses "master 26 invalidates other copies of the target cache line by issuing high-priority Kill transactions" (Page 4, Paragraph 0038)]**.

26. As per **claim 34**, Arimilli discloses "A method comprising: migrating a line of data cache ordering point for a line of data from a first node of a system to a second node of a system; and issuing an invalidate line command for the line of data from the second node to other nodes of the system in response to receiving a conflict response from at least one other node in the system and to the cache ordering point migrating from the first node to the second node" **[The rationale of claim 1 is herein incorporated. Arimilli further discloses "a conflict arises if, during interval 160, the master 26 of a second agent 10 (and possibly one or more additional agents 10) develops, or has previously developed and manifests at any time during interval 160 an intention to modify the target cache line" (Page 3, Paragraph 0029) "master 26 invalidates other copies of the target cache line by issuing high-priority Kill transactions... while master 26 is issuing these Kill transactions, the associated snooper 28 provides NACK**

snoop responses to Dclaim transactions of losing masters 26 that did not receive an NACK snoop response" (Page 4, Paragraph 0038)]. Arimilli further explains [**"The one or more shared cache coherency states may optionally include a shared-owner state that designates a single owner of a potentially shared cache line" (Page 2, Par. 0024) and explains that "master 26 of a first agent, for example, processor complex 10a issues a modifying transaction 150a (i.e., Dclaim or RWITM)" (Page 3, Par. 0029) wherein this processor is granted ownership of the cache line and is designated as OWNER or OWNER_CU (See Table III in Page 6) wherein "The RWITM transaction requests that the initiating agent be provided an up-to-date copy of a target cache line and that other agents invalidate their copies of the cache line, if any" (Page 1, Par. 0006); therefore, disclosing "an ownership response comprising a copy of the data"**] and explicitly discloses [**"master 26" in the system receives store requests for cache lines wherein "master 26 handles the store request according to the coherency state associated with the request address in the cache directory 22... if, however, cache directory 22 indicates the target cache line identified by the request address is invalid... master 26 issuing a RWITM transaction on system bus 12 to obtain a copy of the cache line from another agent 10 for modification" (Page 4, Par. 0035); therefore, as master issues a "RWITM" transaction for data and data is transferred from an agent that has previously modified a cache line to the agent that intends to modify this cache line in order to provide this agent requesting ownership the most-current data in the system, master is issuing an ownership response request comprising a copy of the data as claimed by Applicant**].

27. As per **claim 35**, Arimilli discloses the method of claim 34, **[See rejection to claim 34 above]** further comprising: "providing a first conflict response from the second node to requests for the line of data from the other nodes of the system prior to the cache ordering point migrating from the first node to the second node; and providing a second conflict response from the second node to requests for the line of data from the other nodes after the cache ordering point migrates from the first node to the second node" **[The rationale of claim 18 is herein incorporated]**.

28. As per **claim 36**, Arimilli discloses the method of claim 35, **[See rejection to claim 35 above]** further comprising: "enabling a shared copy of the line of data to be filled at one of the other nodes of the system in response to receiving the first conflict response from the second node and a data response from at least another node of the system; and enabling a copy of the line of data received from system memory to be filled at one of the other nodes of the system in response to receiving the first conflict response from the second node" **[Arimilli discloses this concept as "data associated with a target address are cached at a first agent among the plurality of agents in a shared state... a coherency decision point provides a snoop response granting the first agent ownership of the data... the first agent is permitted to modify the data... to maintain coherency, the first agent also invalidates other cached copies of the data... the coherency decision point at the first agent preferably protect the first agent's ownership of the data by providing appropriate snoop responses to conflicting transactions" (Pages 1-2, Paragraphs 0012-0013)]**.

29. As per **claim 37**, Arimilli discloses the method of claim 35, **[See rejection to claim 35 above]** further comprising "enabling a shared copy of the line of data to be filled at least one of the other nodes of the system for a single use by the at least one of the other nodes of the system

in response to receiving the second conflict response from the first node" **[The rationale of claim 9 is herein incorporated]**.

30. As per **claim 39**, Arimilli discloses "A method comprising: providing a first conflict response from a first node to source broadcast requests for data from other nodes while a source broadcast request for the data is pending at the first node; and providing a second conflict response from the first node to the other source broadcast requests for the data from the other nodes in response to receiving a conflict response and an ownership data response at the first node" **[The rationale of claim 31 is herein incorporated]**.

31. As per **claim 40**, Arimilli discloses "A computer system comprising a plurality of nodes, the plurality of nodes employing a cache coherency protocol operative to migrate a cache ordering point for a line of data from a target node to a source node in response to a source broadcast read request for the line of data issued by the source node, the source node being operative to invalidate the line of data at other nodes of the computer system in response to receiving a conflict response and migratory data to the source broadcast read request" **[The rationale of claim 34 is herein incorporated]**.

Claim Rejections - 35 USC § 103

32. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

33. **Claims 10-11, 23-24, 30 and 38** are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli et al. (US 20020129211) in view of Arimilli et al. (US 6,138,218).

34. As per **claims 10, 23, 30 and 38**, Arimilli discloses the system of claims 8, 21, 26 and 35 **[See rejection to claims 8, 21, 26 and 35 above]** further comprising "a second node that provides one of the other source broadcast requests for the data and receives the second response from the first node," as **[Arimilli discloses this concept as "if snooper 28 determines that the target cache line is invalid in cache directory 22 and that the Dclaim pending flag of the associated master 26 is set, snooper 28 belongs to an agent 10 whose master 26 lost arbitration for ownership of the target cache line... snooper 28 therefore provides a RETRY SR" (Page 5, Paragraphs 0043-0045)]**

Arimilli (US 2002/0129211) does not disclose expressly "the second node being operative to employ a forward progress technique to obtain the data."

Arimilli (US 6,138,218) discloses "the second node being operative to employ a forward progress technique to obtain the data" **[Column 6, lines 39-45 and 54-64]**.

Arimilli et al. (US 2002/0129211) and Arimilli et al. (US 6,138,218) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the multiprocessor memory system that provides broadcast/snoops requests to maintain data coherency as taught by Arimilli (US 2002/0129211) and further employ a forward progress technique to obtain the data when broadcasts/snooping are not successful as taught by Arimilli (US 6,138,218).

The motivation for doing so would have been because Arimilli (US 6,138,218) discloses employing a forward process technique to resolve the transaction if the source broadcast/snooping protocol cannot provide a deterministic resolution of the transaction **[(Column 6, lines 39-45 and 54-64)]** to obviate the need for subsequent interventions or snoop/broadcast retries **[(Column 6, lines 48-50)]**.

Therefore, it would have been obvious to combine Arimilli et al. (US 6,138,218) with Arimilli et al. (US 2002/0129211) for the benefit of creating a memory sytem to obtain the invention as specified in claims 10, 23, 30 and 38.

35. As per **claims 11 and 24**, the combination of Arimilli (US 2002/0129211) and Arimilli et al. (US 6,138,218) discloses the system of claims 10 and 23, **[See rejection to claims 10 and 23 above]** wherein "the forward progress technique comprises a forward progress cache coherency protocol" **[The rationale in the rejection of claim 10 is herein incorporated]**.

36. **Claim 15** is rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli et al. (US 2002/0129211) in view of Arimilli et al. (US 6,138,218) and Martin et al. (US 6,883,070).

37. As per **claim 15**, Arimilli (US 20020129211) discloses the system of claim 1, **[See rejection to claim 1 above; the rationale of claim 1 is herein incorporated]** wherein "the first node employs a source broadcast-based protocol to issue the source broadcast request for the data," **[Arimilli** (US 20020129211) **discloses this concept as agents snoop to use resources (Pages 1-2, Paragraphs 0011-0012; Figure 4)]** but does not disclose expressly implementing "a hybrid cache coherency protocol the first node employing an associated forward progress protocol to reissue a request for the data in response to the request failing in the source broadcast protocol."

Arimilli (US 6,138,218) discloses "the second node being operative to employ a forward progress technique to obtain the data to reissue a request for the data in response to the request failing in the source broadcast protocol" **[Column 6, lines 39-45 and 54-64]** but does not disclose expressly using a hybrid cache coherency protocol.

Martin discloses a multi-processor system comprising at least one node that employs a hybrid coherency protocol, the hybrid coherency protocol employing a forward progress protocol to resolve the transaction **[(Abstract; Column 1, lines 38-50)]**.

Arimilli et al. (US 2002/0129211), Arimilli et al. (US 6,138,218) and Martin et al. (U 6,883,070) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the multiprocessor memory system that provides broadcast/snoops requests to maintain data coherency as taught by Arimilli (US 2002/0129211); employ a forward progress technique to obtain the data when broadcasts/snooping are not successful as taught by Arimilli (US 6,138,218) and further use a hybrid cache coherency protocol as taught by Martin.

The motivation for doing so would have been because Arimilli (US 6,138,218) discloses employing a forward process technique to resolve the transaction if the source broadcast/snooping protocol cannot provide a deterministic resolution of the transaction **[(Column 6, lines 39-45 and 54-64)]** to obviate the need for subsequent interventions or snoop/broadcast retries **[(Column 6, lines 48-50)]** and Martin discloses **[using a hybrid coherency protocol employing a forward process protocol to provide a hybrid protocol that**

is sensitive to the bandwidth available for communication of cache protocol messages (Column 2, lines 27-30)].

Therefore, it would have been obvious to combine Martin et al. (US 6,883,070), Arimilli et al. (US 6,138,218) with Arimilli et al. (US 2002/0129211) for the benefit of creating a memory system to obtain the invention as specified in claim 15.

ACKNOWLEDGMENT OF ISSUES RAISED BY THE APPLICANT

Response to Amendment

38. Applicant's arguments filed December 20, 2006 have been fully considered but they are not deemed to be persuasive as required by **M.P.E.P. § 707.07(f)**, a response to these arguments appears below.

ARGUMENTS CONCERNING PRIOR ART REJECTIONS

39. Claims must be given the broadest reasonable interpretation during examination and limitations appearing in the specification but not recited in the claim are not read into the claim (See M.P.E.P. 2111 [R-1]).

1ST POINT OF ARGUMENT

40. In response to applicant's remark that Arimilli does not disclose a first node that provides a source broadcast request for data since such data is already at the master that issues the transaction; the Examiner disagrees as **[Arimilli discloses "processor complex 10a-10n" (Figure 1) which corresponds to different nodes in the system and explains that "process complex 10a, issues a modifying transaction 150a (i.e., Dclaim or RWITM) on system bus**

12 that targets a cache line that is indicated as shared in the cache directory 22 of at least one agent 10" (Par. 0029) wherein "The RWITM transaction requests that the initiating agent be provided an up-to-date copy of a target cache line and that other agents invalidate their copies of the cache line, if any" (Page 1, Par. 0006)| which one of ordinary skill in the art would readily recognize as a source broadcast request for data in a shared cache memory system.

2ND POINT OF ARGUMENT

41. Applicant argues that Arimilli does not disclose first and second manners of responding as Arimilli states that the CDP, not the first agent protects the grant of ownership until the combined response is received at the first agent. The examiner disagrees and would like to respectfully point out that this argument does not patentably distinguish the current Application from Arimilli. Armilli discloses "the first node being operable to respond in a first manner to other source broadcast request for the data while the source broadcast request for the data is pending at the first node" as **|processor 10a issues modifying transaction 150a while, during interval 160, other processors issue conflicting responses 150b, 150c and 150e and CDP (agent that holds the data in the highest state of ownership) grants ownership of the target cache line to an agent 10 which is designated as the next CDP (Page 3, Pars. 0029-0031) and explains that "ownership of the target cache line by processor complex 10a is protected by the granting CDP during interval 162... Following interval 162, that is, during interval 164 between receipt of a combined response 154a and the close of interval 160, processor complex 10a can protect its ownership by providing snoop responses" (Pages 3-4, Par. 0033; Figures 1 and 2). Furthermore, Arimilli clearly explains that "ideally, processor complex 10a would "know" immediately after issuing modifying transaction 150a that it**

will be awarded ownership and would be able to protect its ownership by providing snoop responses denying ownership to the agents 10 that issued conflicting transactions" (Page 3, Par. 0033); thereby, one of ordinary skill in the art would readily recognize that Applicant's argument does not patentably distinguish the current Application from Arimilli].

Arimilli also discloses "the first node being operable to respond in a second manner to other source broadcasts for the data in response to receiving an ownership data response" **as ["master 26 prevents access to the target cache line by other agents 10 by means of appropriate snoop responses until the store into cache array 24 is completed" (Page 4, Par. 0036). Applicant is also respectfully directed to Table I (Page 5) and Table III (Page 6) which provide a list of possible ownership responses by nodes in the system].**

3RD POINT OF ARGUMENT

42. With respect to Applicant's remark that Arimilli does not disclose that an ownership data response includes a copy of the data; Applicant is reminded that the claims are given the broadest reasonable interpretation and limitations found in the Specification but not in the claims are not read into the claims. Arimilly disclose that an ownership data response includes a copy of the data as **["The one or more shared cache coherency states may optionally include a shared-owner state that designates a single owner of a potentially shared cache line" (Page 2, Par. 0024) and explains that "master 26 of a first agent, for example, processor complex 10a issues a modifying transaction 150a (i.e., Dclaim or RWITM)" (Page 3, Par. 0029) wherein this processor is granted ownership of the cache line and is designated as OWNER or OWNER_CU (See Table III in Page 6) wherein "The RWITM transaction requests that the**

initiating agent be provided an up-to-date copy of a target cache line and that other agents invalidate their copies of the cache line, if any" (Page 1, Par. 0006); therefore, disclosing "an ownership response comprising a copy of the data"].

Arimilli explicitly discloses **["master 26" in the system receives store requests for cache lines wherein "master 26 handles the store request according to the coherency state associated with the request address in the cache directory 22... if, however, cache directory 22 indicates the target cache line identified by the request address is invalid... master 26 issuing a RWITM transaction on system bus 12 to obtain a copy of the cache line from another agent 10 for modification" (Page 4, Par. 0035); therefore, as master issues a "RWITM" transaction for data and data is transferred from an agent that has previously modified a cache line to the agent that intends to modify this cache line in order to provide this agent requesting ownership the most-current data in the system, master is issuing an ownership response request comprising a copy of the data as claimed by Applicant].**

4TH POINT OF ARGUMENT

43. With respect to Applicant's remark that Arimilli does not disclose that the ownership data response comprises an indication to the first node that the data associated with the ownership data response comprises migratory data; the Examiner disagrees. Applicant's Specification defines "migratory data" (Paragraph 0024) as memory blocks shared by a plurality of processors and explains that if a read finds data is modified by another processor, it must migrate data to this processor and move a cache ordering point to this processor (Paragraph 0027) which Arimilli discloses as **["master 26 handles the store request according to the coherency state associated with the request address in the cache directory 22... if, however, cache directory**

22 indicates the target cache line identified by the request address is invalid... master 26 issuing a RWITM transaction on system bus 12 to obtain a copy of the cache line from another agent 10 for modification" (Page 4, Par. 0035)].

5TH POINT OF ARGUMENT

44. In response to Applicant's remark that Arimilli does not disclose a cache ordering point for serializing source broadcast requests for the data. Applicant's Specification defines a cache ordering point as an owner processor or node serves as a cache ordering point wherein the owner processor responds to other processor with data to snoops for the data (Par. 0027) **["master 26 handles the store request according to the coherency state associated with the request address in the cache directory 22... if, however, cache directory 22 indicates the target cache line identified by the request address is invalid... master 26 issuing a RWITM transaction on system bus 12 to obtain a copy of the cache line from another agent 10 for modification" (Page 4, Par. 0035); therefore, as the copy of the valid data is transferred to the owning processor comprises a cache ordering point, as claimed by Applicant]**.

6TH POINT OF ARGUMENT

45. Applicant argues that "claim 8 has been amended to make explicit that which was previously implicit;" however it is noted that claim 8 has not been amended. **[Refer to the rejection to claim 8 above]**.

7TH POINT OF ARGUMENT

46. Applicant argues Arimilli does not disclose "employing a copy of data for a single use;" however, the Examiner disagrees **[Refer to the rejection to claim 9 above]**. Furthermore, according to the broadest reasonable interpretation given to the claims term "a single use"

comprises any use and Arimilli clearly discloses **["coherency protocols typically require that only a single agent can own each line at any given time for purposes of modification" (Page 3, Paragraph 0033)]** wherein "modification" comprises a single use.

8TH POINT OF ARGUMENT

47. Applicant argues Arimilli fails to teach the source processor node issues an invalidate line command to other processor nodes of the system in response to receiving a data response that transfers the copy of the data; the Examiner disagrees as Arimilli discloses an ownership response that transfers the copy of the data **[See third point of argument above]** and also discloses **["in addition, to maintain coherency, master 26 performs clean-up operations to invalidate other (now stale) copies of the target cache line, if any, held by other agents 10" (Page 4, Par. 0038)]**.

8TH POINT OF ARGUMENT

48. Regarding Aplicant's remark that one of ordinary skill in the art would not be motivated to combine Arimilli with the forward progress protocol of Arimilli 218 because Arimilli does not teach other source broadcast requests for the data or that the second node is operative to obtain the data; the Examiner disagrees **[Refer to 1st and 3rd points of argument above]** where it is disclosed that one node obtains data previously modified at another node.

Furthermore, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and In re Jones, 958 F.2d 347, 21

USPQ2d 1941 (Fed. Cir. 1992). In this case, both Arimilli and Arimilli 218 are directed to and involved in shared memory systems access and control. **[Motivation to combine these references can be found in rejection to claims 10, 23, 30 and 38 above]**.

9TH POINT OF ARGUMENT

49. In response to Applicant's arguments that one of ordinary skill in the art would not be motivated to combine the system or Arimilli with Arimilli 218 and Martin to create the system of claim 15 as Martin provides no suggestion of the ability to switch between protocols as recited in claim 15; the Examiner disagrees with Applicant's arguments as Arimilli 218 is relied upon for switching between protocols **[(Col. 6, lines 39-45 and 54-64; Refer to rejection to claim 15 above)]**. The reference to Martin has only been relied upon for teaching a multiprocessor system using a hybrid cache coherency protocol **[Abstract; Col. 1, lines 38-50]**.

Furtheremore, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Arimilli, Arimilli 218 and Martin are directed to and involved in shared memory systems access and control. **[Motivation to combine these references can be found in rejection to claim 15 above]**.

50. All arguments by the applicant are believed to be covered in the body of the office action or in the above remarks and thus, this action constitutes a complete response to the issues raised in the remarks dated December 20, 2006.

CLOSING COMMENTS

Examiner's Note

51. Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant, in preparing the responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

Conclusion

52. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

53. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

STATUS OF CLAIMS IN THE APPLICATION

54. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. § 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

55. Per the instant office action, **claims 1-40** have received a second action on the merits and are subject of a final rejection.

DIRECTION OF ALL FUTURE REMARKS

56. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yaima Campos whose telephone number is (571) 272-1232. The examiner can normally be reached on Monday to Friday 8:30 AM to 5:00 PM.

IMPORTANT NOTE

57. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Sanjiv Shah, can be reached at the following telephone number: Area Code (571) 272-4098.

58. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions

on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

March 26, 2007

Yamna Campos
Examiner
Art Unit 2185

SANJIV SHAH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100